

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Currently amended) A clock synchronization circuit for generating an in-synchronization signal that indicates an in-synchronization state wherein an delayed output clock signal ~~that is substantially in synchronization with a reference clock signal when in an in-synchronization state with a phase difference between the two clock signals of less than a predetermined value,~~ the clock synchronization circuit comprising:
 - a programmable delay element coupled to the reference clock signal for introducing an adjustable delay in the reference clock signal to produce a delay-adjusted delayed output clock signal that becomes increasingly closer to being in synchronization with the reference clock signal; and
 - a phase detector coupled to the reference clock signal and the delay-adjusted delayed output clock signal for detecting the phase difference between the two clock signals and for generating ~~an the~~ in-synchronization signal when the in-synchronization state is reached;
 - wherein the in-synchronization signal is a pulse having a pulse width sufficient to interrupt a microprocessor, and the in-synchronization state is reached when the phase difference between the reference clock signal and the delay-adjusted delayed output clock signal is less than a predetermined value.

3. (Previously amended) A clock synchronization circuit for generating an output clock signal that is substantially in synchronization with a reference clock signal when in an in-synchronization state with a phase difference between the two clock signals of less than a predetermined value, the clock synchronization circuit comprising:

a programmable delay element coupled to the reference clock signal for introducing an adjustable delay in the reference clock signal to produce a delay-adjusted delayed output clock signal that becomes increasingly closer to being in synchronization with the reference clock signal; and

a phase detector coupled to the reference clock signal and the delay-adjusted delayed output clock signal for detecting the phase difference between the two clock signals and for generating an in-synchronization signal when the in-synchronization state is reached, the phase detector comprising:

a pulse generator that produces a pulse of variable width when the output clock signal approaches the in-synchronization state as the adjustable delay is increased; and

a latch that is triggered by the pulse to generate the in-synchronization signal when the width of the pulse reaches a pulse width Z required to trigger the latch.

4. (Original) A clock synchronization circuit according to Claim 3, wherein the latch is a D-type latch.

5. (Original) A clock synchronization circuit according to Claim 3, wherein the pulse generator comprises:

means for producing a window of a known width Y that is at least equal to the pulse width Z ; and

means for generating a signal (IN1) from the delay-adjusted delayed output clock signal whose mark of a cycle is brought to overlap with the window when the adjustable delay is increased to produce the pulse.

6. (Previously amended) A clock synchronization circuit according to Claim 5, wherein the means for producing the window is a three-input AND gate having a first input coupled to the generated signal (IN1), wherein the generated signal is the reference clock signal delayed substantially by $2Y$, a second input coupled to the reference clock

signal, and a third input coupled to the reference clock signal that is inverted and delayed by at least Y.

7. (Previously amended) A clock synchronization circuit according to Claim 6, wherein the in-synchronization state is reached when the pulse width of the pulse generated by the pulse generator reaches a width $Y-X$ that is equal to the pulse width Z; whereby the in-synchronization signal is generated, wherein X is a phase difference between the reference clock signal and the output clock signal.

8. (Previously amended) A clock synchronization circuit according to Claim 6, wherein the third input of the three-input AND gate is coupled to the reference clock signal that is inverted and delayed by $Y+D$, whereby D is a delay provided by a delay element.

9. (Original) A clock synchronization circuit according to Claim 8; wherein the bounds of the phase difference X is given by a worst case phase lead of $Y_{\max}-Z_{\min}$ and a worst case phase lag of $Y_{\min}-Z_{\max}$ depending on the values of Y and Z, wherein

Y_{\max} and Y_{\min} are the maximum and minimum delays of a NOT gate respectively; and

Z_{\max} and Z_{\min} are the maximum and minimum pulse widths required to trigger the latch respectively.

10. (Previously amended) A clock synchronization circuit according to Claim 2, wherein the clock synchronization circuit is implemented in a programmable gate array.

11. (Original) A clock synchronization circuit according to Claim 8, wherein the delay-adjusted output clock signal is carried on a trace on a printed circuit board on which the programmable gate array is mounted.

12. (Previously amended) A method of generating a delayed output clock signal that is substantially in synchronization with a reference clock signal when the delayed output

clock signal has a predetermined phase difference X with the reference clock signal, the method comprising:

inverting and delaying by a first delay the reference clock signal to produce an intermediate clock signal, wherein this intermediate clock signal cooperates with the reference clock signal to provide a window of width equal to the predetermined delay;

introducing an adjustable delay in the intermediate clock signal to produce a delay-adjusted delayed output clock signal;

inverting and delaying by a second predetermined delay Y the delay-adjusted delayed output clock signal to produce the reference clock signal delayed by the first delay and the second predetermined delay Y ;

increasing the adjustable delay to bring a cycle of the delay-adjusted delayed output clock signal to be increasingly in synchronization with a subsequent cycle of the reference clock signal until a synchronization condition is reached where a mark of a cycle of the reference clock signal delayed by the first delay and the second predetermined delay Y appears in the window to indicate that the delay-adjusted delayed output clock signal leads the reference clock signal by the phase difference X that is equal to the second predetermined delay Y .

13. (Original) A method according to Claim 12, wherein increasing the adjustable delay comprises increasing the adjustable delay by a known delay step D each time the adjustable delay is incremented.

14. (Previously amended) A method according to Claim 13, further comprising increasing the delay by a further number of delay steps corresponding to Y/D to bring the delay adjusted delayed output clock signal to be more in synchronization with the reference clock signal after the synchronization condition is reached.

15. (Original) A method according to Claim 12, wherein increasing the adjustable delay comprises increasing the adjustable delay until a portion of the mark corresponding

to a width of Z appears in the window; whereby the delay-adjusted delayed output clock signal leads the reference clock signal by a phase difference X that is equal to the second predetermined delay Y minus the width Z .

16. (Original) A method according to Claim 13, wherein Y is smaller than Z and the first delay is greater than Z and wherein increasing the adjustable delay comprises increasing the adjustable delay until a portion of the mark corresponding to a width of Z appears in the window; whereby the delay-adjusted delayed output clock signal lags the reference clock signal by a phase difference X that is equal to the width Z minus the second predetermined delay Y .